ABSTRACT

A power component formed in an N-type silicon substrate delimited by a P-type wall, having a lower surface including a first P-type region connected to the wall, and an upper surface including a second P-type region, a conductive layer extending above the substrate between the second region and the wall. The component includes a third N-type region of high doping level formed in the substrate under the portion of the layer substantially halfway between the external periphery of the second region and the internal periphery of the wall. This third region is contacted by a field plate extending on either side of the third region in the direction of the wall and of the third region.